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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,608	07/23/2004	Kangguo Cheng		4607

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EXAMINER
REAMES, MATTHEW L

ART UNIT	PAPER NUMBER
2891	

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01/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/710,608	**Applicant(s)** CHENG ET AL.	
	Examiner Matthew L. Reames	**Art Unit** 2891	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 17 December 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☐ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented: See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: see attached.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/17/2007 have been fully considered but they are not persuasive. Applicant argues Peterson does not teach a device in the strained layer and a device relaxed layer and merely teaches a patterned substrate.

2. .Peterson states:

> "For example, strained and relaxed structures are used during fabrication of an integrated device in creating high-speed complementary metal-oxide semiconductor (CMOS) circuitry. Positive channel metal-oxide semiconductor (PMOS) devices with compressively strained layers (e.g. SiGe or SiGeC channels) have the desirable quality of being faster than their silicon counterparts. However, the opposite is true of compressively strained SiGe negative channel metal-oxide semiconductor (NMOS) devices; they are slower than their silicon counterparts. In order to obtain fast NMOS devices, strained Si channels are fabricated over a relaxed (e.g. SiGe or SiGeC) layer (also known as a buffer layer). The integration of both of these types of devices on a common substrate, however, requires that both strained and relaxed SiGe (or SiGeC) layers be present on that substrate. Unfortunately, current fabrication techniques do not allow the simultaneous fabrication of both strained and relaxed crystalline, poly-crystalline, and amorphous structures using common fabrication steps.

Hence, what is needed is a method for co-fabricating strained and relaxed crystalline, poly-crystalline, and amorphous structures without the problems described above."

Further Peterson teaches the objective is to:

"The present invention relates to the process of fabricating integrated devices. More specifically, the present invention relates to a method for co-fabricating strained and relaxed crystalline, poly-crystalline, and amorphous structures during integrated device fabrication."

3. Peterson is teaching a method to overcome the limitations of the prior so that one can build PMOS and NMOS on the same substrate. One in and on a strained material and the other in a relaxed. Therefore Peterson teaches a channel of the transistor in a strained layer (PMOS) and a channel (NMOS) in the relaxed layer. Therefore Peterson teaches using this patterned substrate for use with PMOS NMOS with a patterned substrate.

4. Applicant further argues that the devices are not formed in the material. This is not found convincing since Peterson teaches the channel in the strained and relaxed layer (see paragraph 7). Further Applicant is invited to review their IDs for the disclosure of how NMOS and PMOS are formed.

5. Lastly Applicant argues that the Peterson does not teach a strained device or a relaxed device. This is not found convincing since applicant teaches that transistors (PMOS or NMOS) maybe either be strained or relaxed devices. Since the channel of

the PMOS is formed in the strained layer the device is strained due to the the channel being strained. A similar argument can be made for the NMOS since the channel is formed in the relaxed layer.

6. Therefore all rejections are deemed proper and maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew L. Reames whose telephone number is (571)272-2408. The examiner can normally be reached on M-Th 6:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, B. William Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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